

REMARKS

Claims 1-20 are pending and stand rejected by the examiner.

Applicants have added new claims 21-25. No new matter was added.

The examiner rejected claims 1-20 as failing to comply with the enablement requirement.

More specifically, the examiner finds no support for concatenating, shifting and storing in a single clock cycle.

Applicants have cancelled claims 2, 3, 9 and 10, added new independent claim 21, and amended independent claims 1 and 8 to comply with the enablement requirement of 35 USC §112, first paragraph. More specifically, claims 1, 8 and 21 recite "in a single cycle in a parallel hardware-based multithreaded processor, concatenating a first 32-bit word and a second 32-bit word to produce a 64-bit intermediate result," or similar language. The quoted feature is supported in the specification as originally filed:

The processor core 20 includes a RISC core 50 implemented in a five stage pipeline performing a single cycle shift of one operand or two operands in a single cycle, provides multiplication support and 32 bit barrel shift support.
(specification page 8, lines 14-16)

Applicants' first 32-bit word and second 32-bit word are two operands. Accordingly, claims 1, 4-8, 11-25 are proper under 35 USC §112, first paragraph.

The fact that the applicants have not responded to any stated position of the Examiner should not be construed as a concession by the applicants of those positions. The inclusion by the applicants of arguments for patentability should not be construed as a concession by the applicants that there are not other good reasons for patentability of these claims or other claims.

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Enclosed is an \$86 check for excess claim fees. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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